SILEXICA

FPGA Accelerators: How to beat RTL design latency with C++ in a fraction of the time

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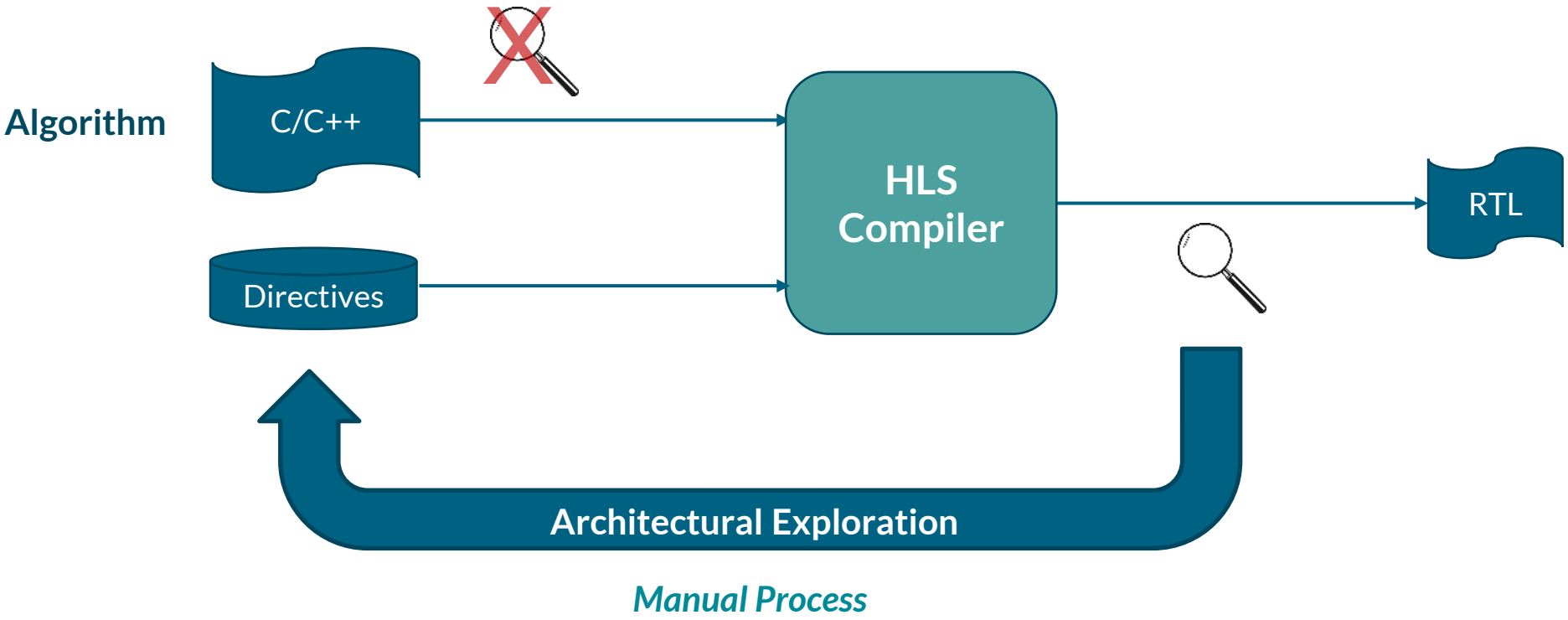
FPGA Acceleration

Long Development Cycles
Designer Scarcity
Limited Toolset

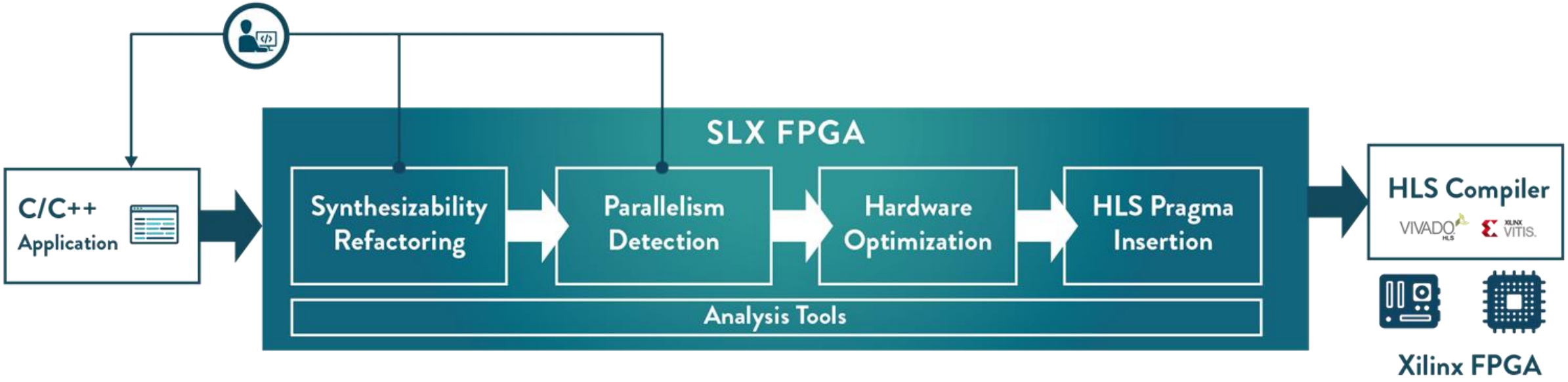
Algorithm Development
(Time to Market)

Latency & Throughput
(Time in Market)

High Level Synthesis (HLS)

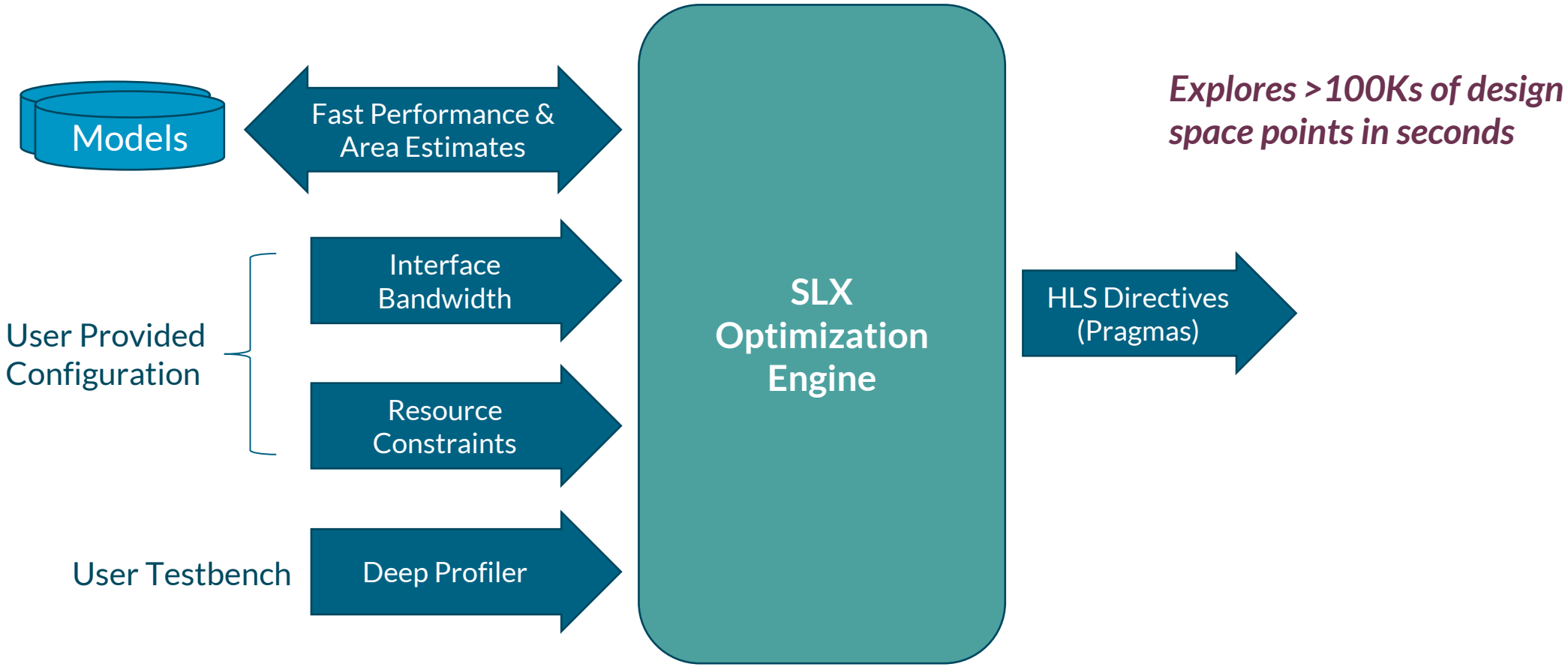


SLX FPGA - Automated Workflow for HLS



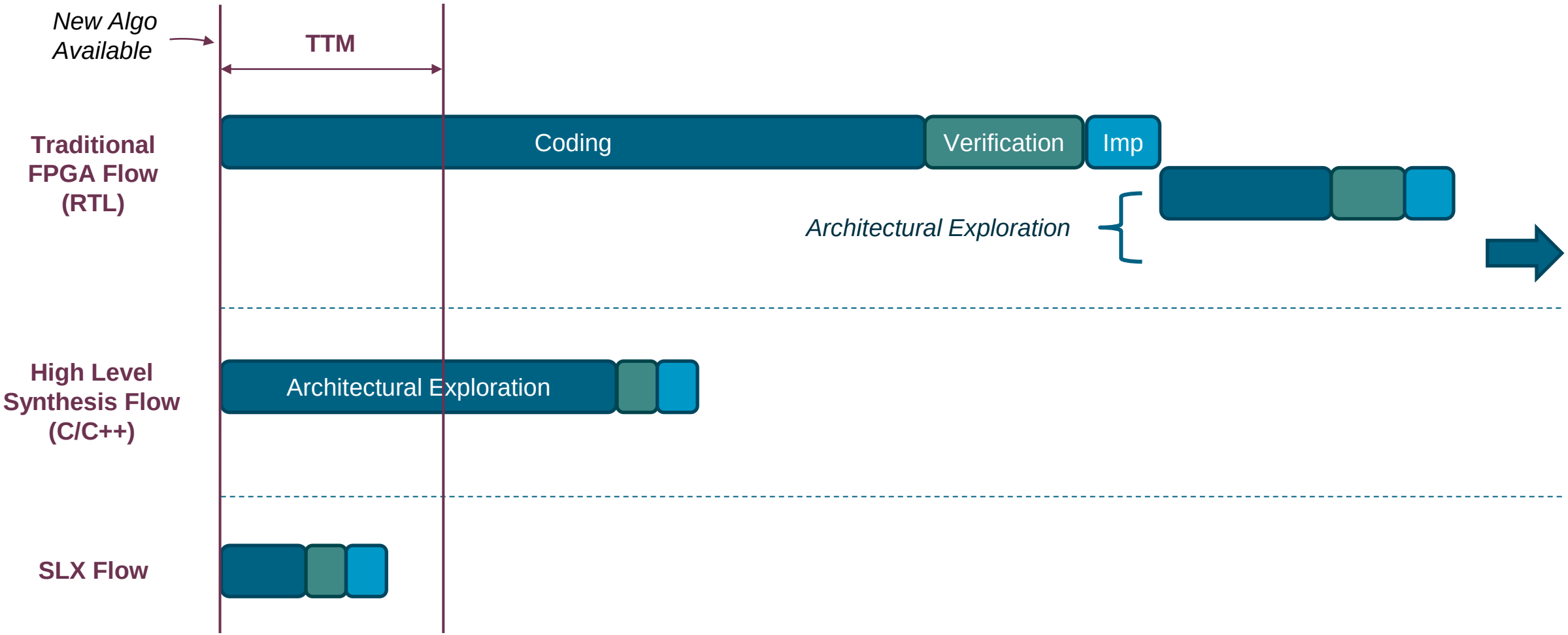
Hot spots
Memory Access Patterns
Data Dependencies

The SLX Automated Optimization Engine



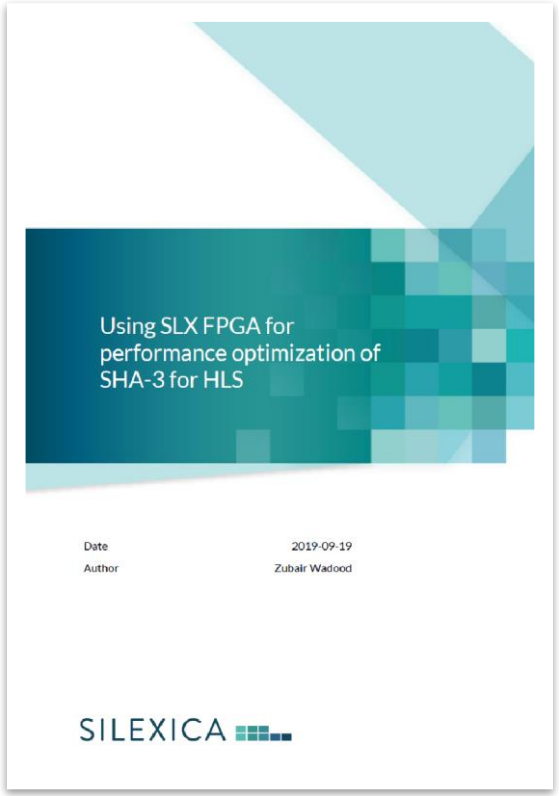
Explores >100Ks of design space points in seconds

Algorithm Development Cycle



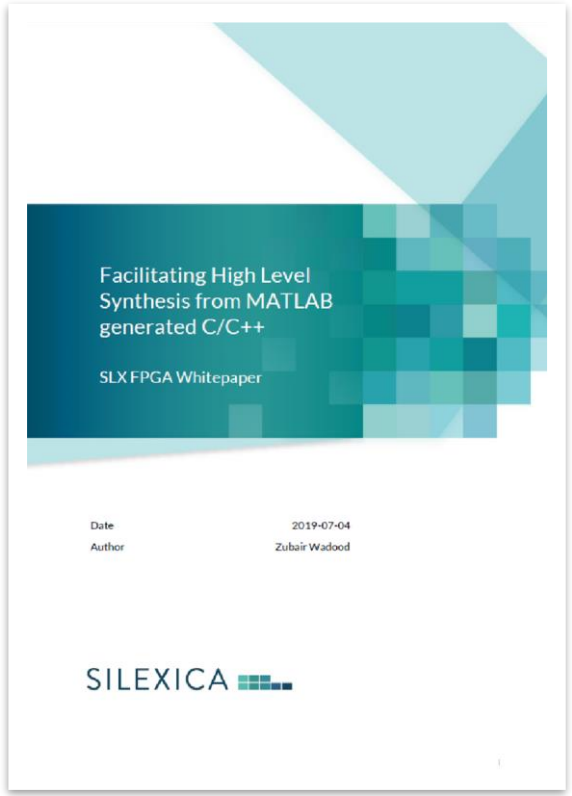
Push button results

Silexica white Papers *(No STAC Benchmark)*
www.silexica.com



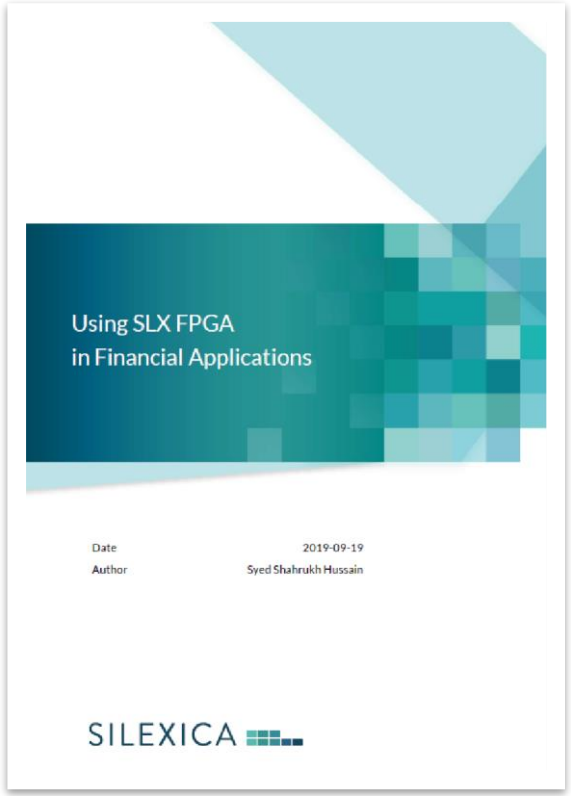
SHA-3 Algorithm, download here

600x Speed-up with SLX FPGA



Kalman Filter, download here

62x Speed-up with SLX FPGA



Black-Scholes & Heston, download here

29x Speed-up with SLX FPGA