Cracking the code on FPGA:

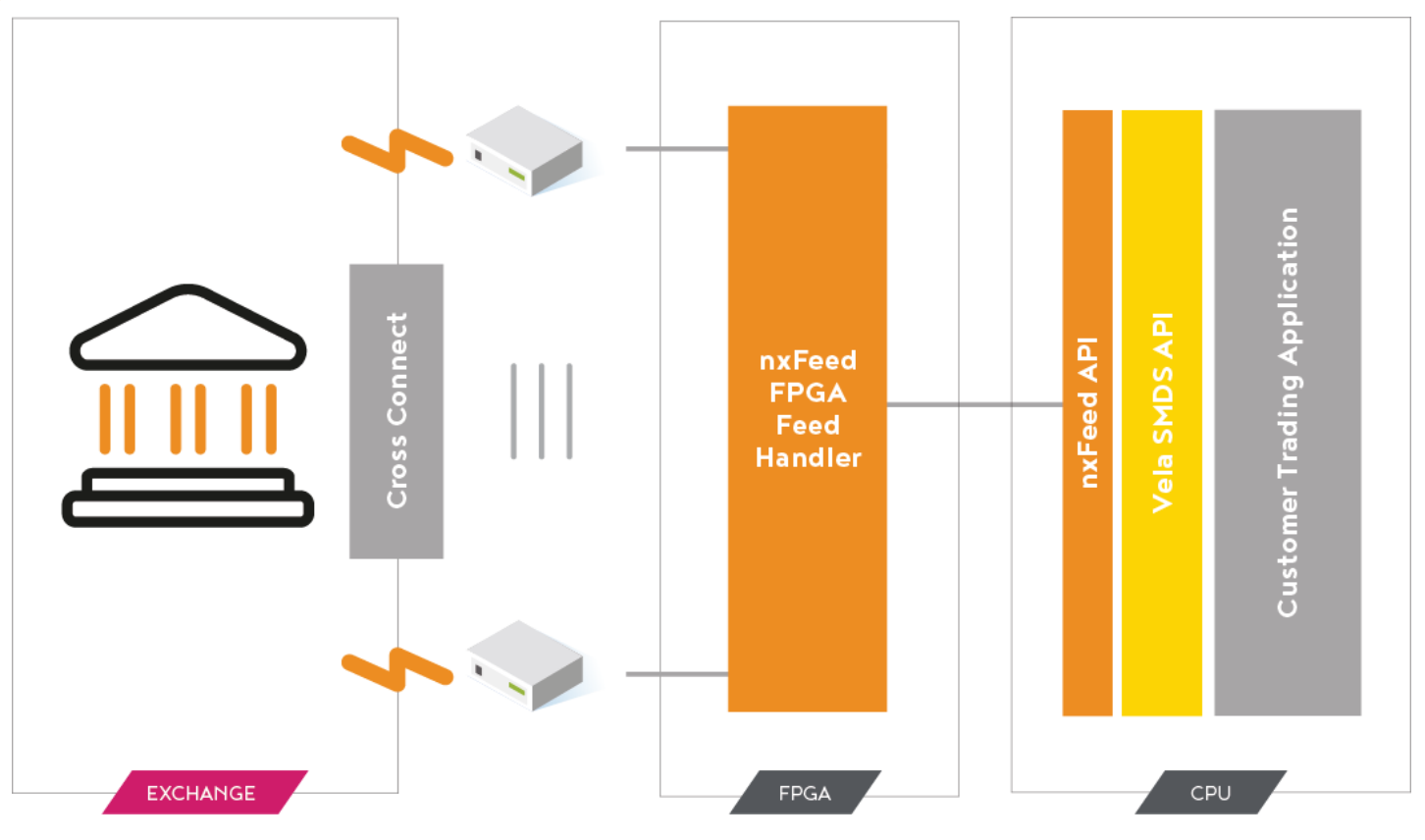
How Enyx is making hardware performance more accessible

Market Data Distribution

- Full featured, full hardware FPGA feed handler:
  - Hardware order management & book building
  - A/B arbitration (supports wireless & fiber feeds)
  - Filtering per symbol, message type, and book depth
  - Supports up to **256 000 Symbols** per FPGA
- Easy integration:
  - Interface with trading application via lean C++ API
  - Standard network connectivity
  - Normalized data available over PCIe and/or Ethernet Multicast
- Performance:
  - **Average Latency of 1µs***
  - **Maximum Latency Under 5µs***
- Supports more than 60 Venues

* Not a STAC benchmark

Vela's FPGA-enabled Ticker Plant:



Hardware Processing:

- Decoding, line arbitration, filtering, and full order management & book building

Software Processing:

- Normalization and distribution

- Can be deployed in any server able to host a PCIe FPGA card

- No application code changes

Performance Without Compromises:

		Full Software Deployment	FPGA Enabled Deployment	Improvement
		**13 Cores** per protocol*	**1 Core** per protocol*	**x 13**
		**4 Units** for a full US Equities deployment*	**2 Units** for a full US Equities deployment*	**x 2**
	**min**	**4.1 µs***	**1.3 µs***	**x 3**
	50%	**6.0 µs***	**2.0 µs***	**x 3**
	max	**904 µs***	**8.9 µs***	**x 100**

* Not a STAC benchmark

FPGA Development Framework

The Enyx Framework is a hardware & software development environment that makes building SmartNIC applications more efficient.

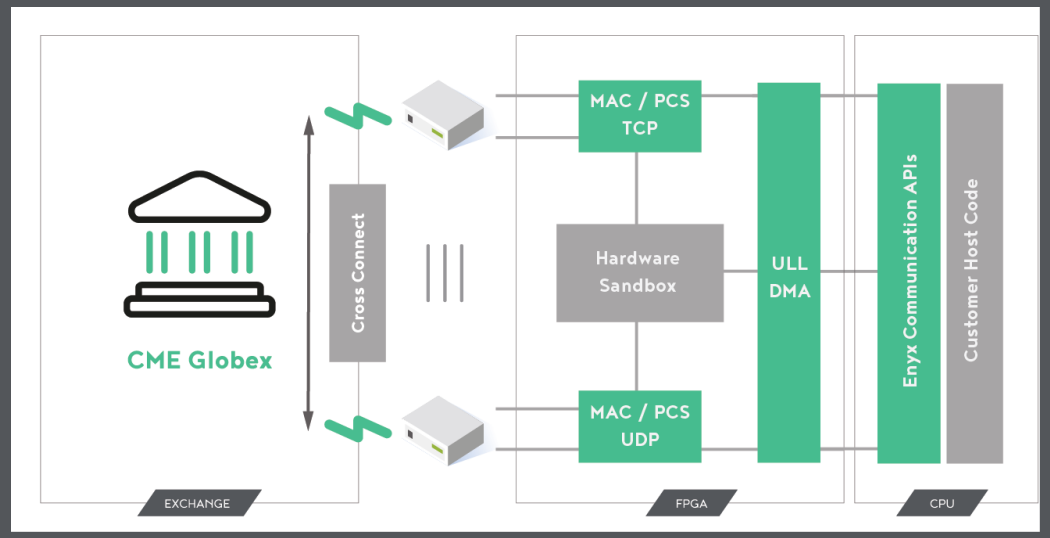
The following IP Cores are provided :

- 10G Ultra Low Latency PCS+MAC (40ns RTT*)
- 10G Full TCP Stack (17ns Tx latency*)
- 1G/10G/25G PCS+MAC, Full TCP/UDP Stacks
- Ultra Low Latency PCIe Streaming DMA
- Board Management cores
  - Flash controller support
  - I²c bus controller
  - Instantiation of memory controllers (DDR4, QDR II+)

- A large support of FPGA families
- Configurable BSP for flexible and scalable deployments
- Linux Driver and low level configuration/communication libraries

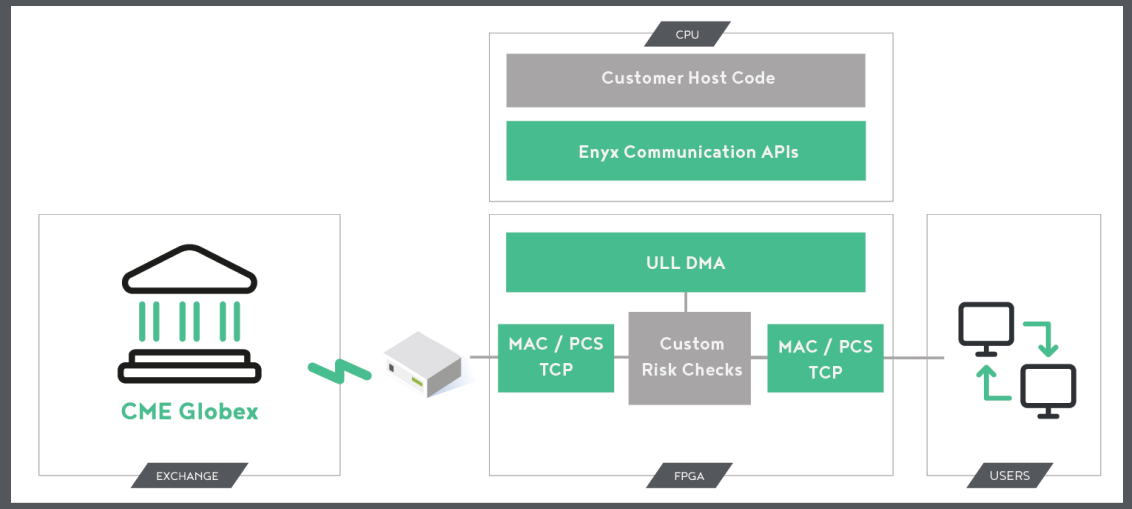
* Not a STAC benchmark

Ultra Low Latency Tick-to-Trade



- Standard reference design for ULL Tick-to-Trade FPGA trading strategies.
- The Enyx development framework provides all the required hardware and software modules to help with the developments.
- **Sub 100ns latency***

Low Latency Risk Check Gateway



- Standard reference design for risk checks gateway acceleration.
- Two distinct TCP stacks connect respectively to the users and to the exchange.
- **Sub 1µs latency***

* Not a STAC benchmark

Technology & IP Cores - Programing Languages

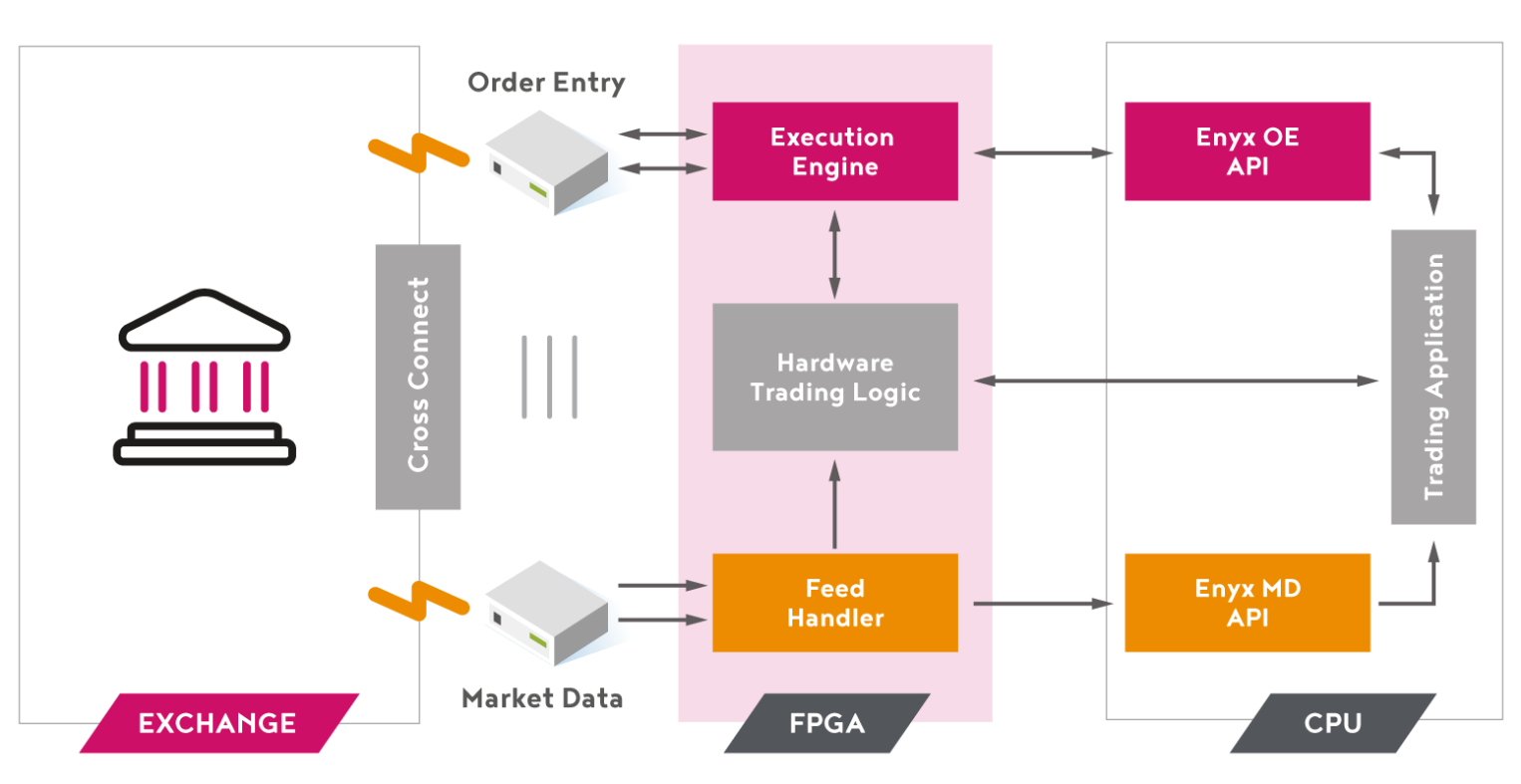
- The Client Business Logic can be developed in:
  - Verilog
  - VHDL
  - Using Vivado HLS in C++
- The software code on the Host can be developed in C or C++.
- All the scripts provided with the framework to manage the flow and build firmwares are developed in Python.

End to End Market Access

- Full featured, full hardware FPGA feed handler
- Full featured, FPGA-enabled execution gateway:
  - Pre-load up to **16 384 orders** or groups of orders in FPGA
  - Full hardware TCP stack
  - In-FPGA Kill Switch & Full Audit-trail
  - Can accelerate API-based execution protocol
- Easy integration:
  - Interface with trading application via **lean C++ API**
  - Standard network connectivity
  - Supports Hardware & Software trading algorithms
  - Hardware algorithm can be develop in either **HDL** or **HLS**
- Performance:
  - Hardware trading logic: **Sub 750ns latency***
  - Software trading logic: **Sub 1.8µs latency***

* Not a STAC benchmark

Hybrid Software & Hardware Trading Algorithm Deployment:



- Both the hardware and software strategy can trigger orders allowing only the critical path to be ported onto the FPGA
- Enyx provides an HLS development kit allowing software engineers to develop their own FPGA-based trading logic
- **Sub 750ns latency***

* Not a STAC benchmark

Code, Documentation and Tutorials available on our website

http://info.enyx.com/contact

Don’t forget to tick the Enyx box for more information