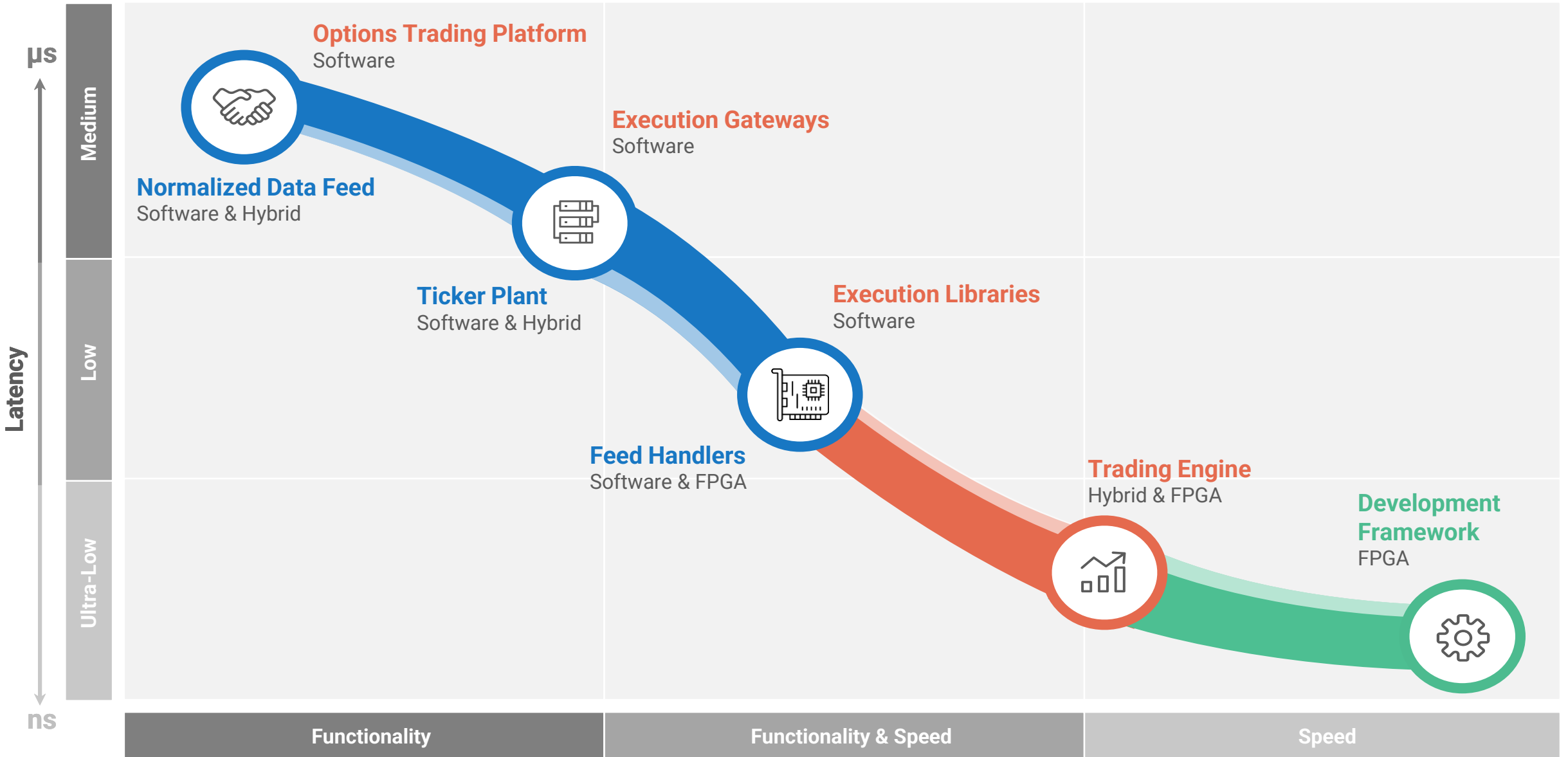




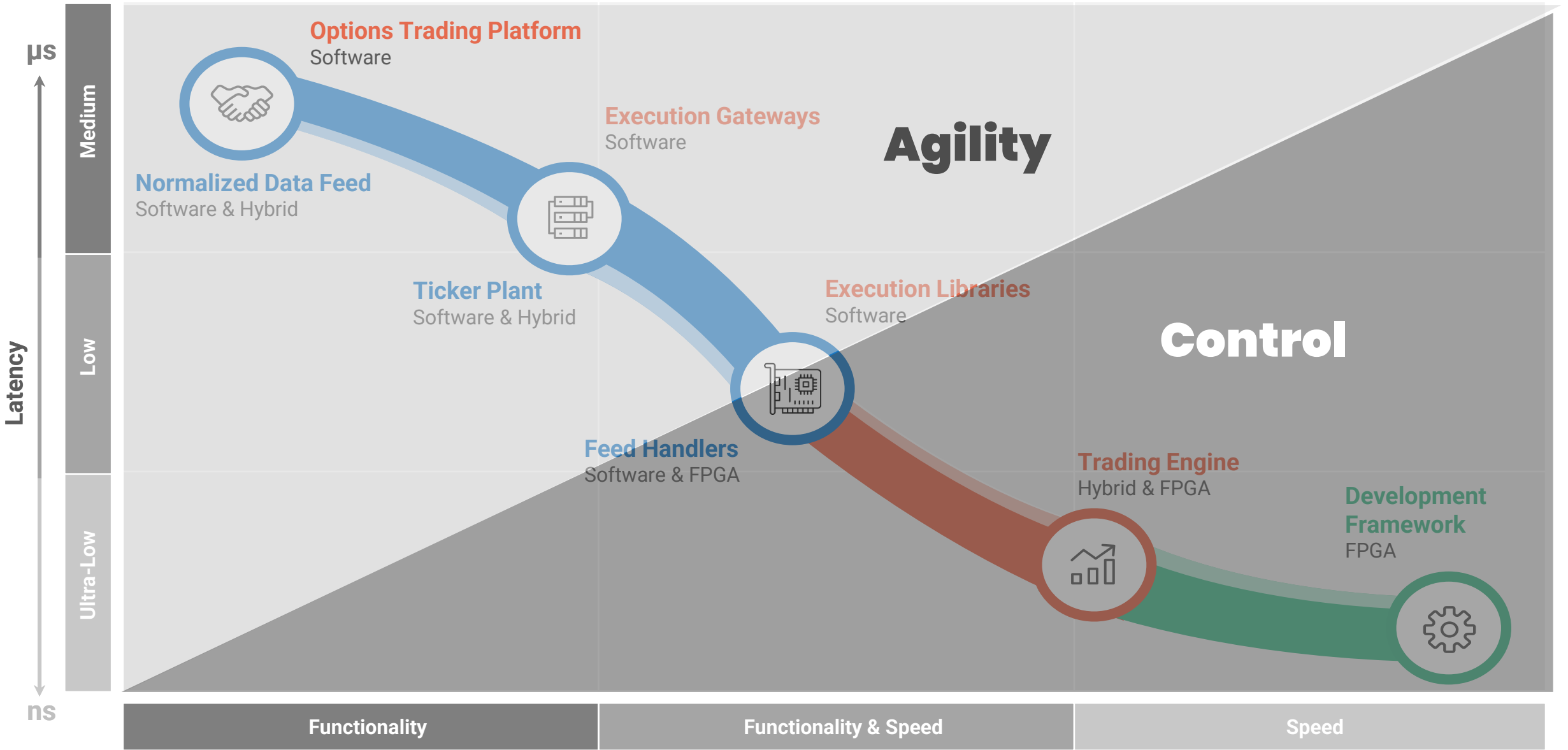
Beyond the Tick: AMD & Exegy's Clockless breakthrough in FPGA Tick-to-Trade Latency

STAC Chicago – May 30, 2024

Where our solutions fit? *The Latency Spectrum*



Control & Agility: Exegy as a strategic partner



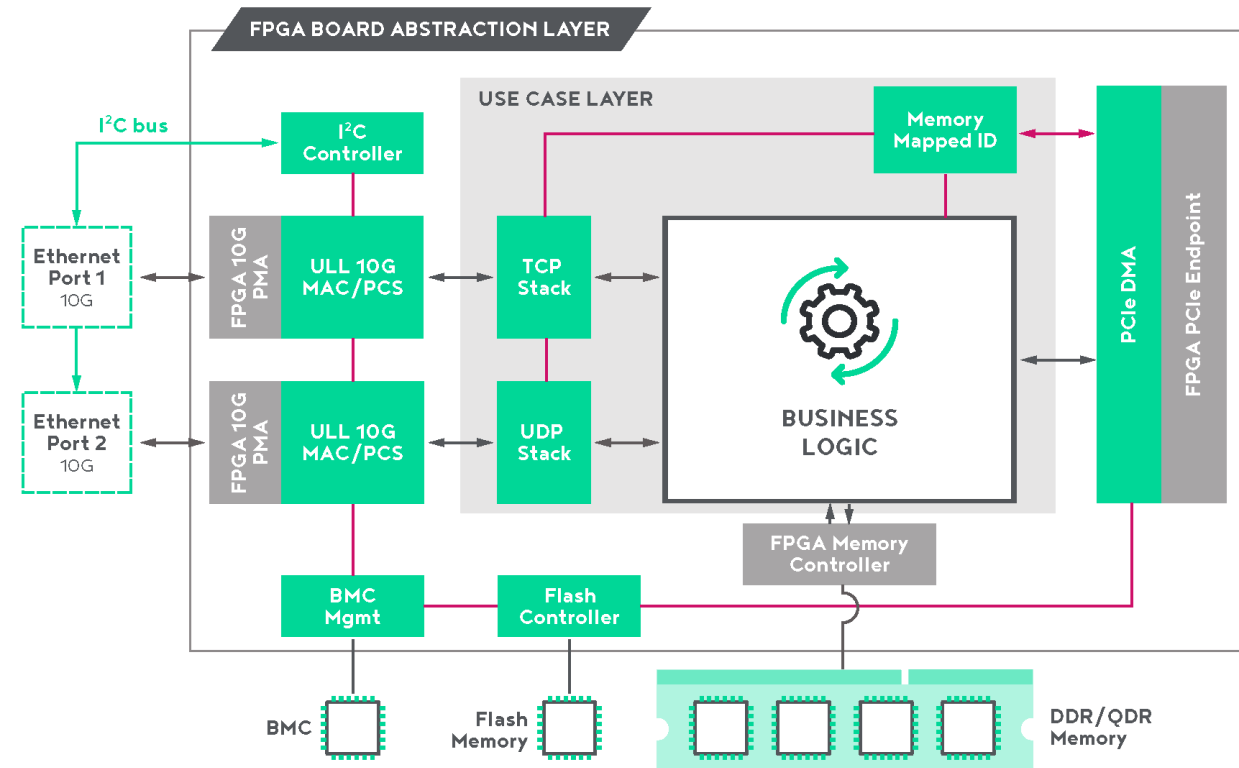
nxFramework – Constantly evolving

» New Application layers

- Risk check with FIX & Native
- Ultra-low latency tick-to-trade
- ARISTA-based designs/applications

» New integrated TCP-UDP-ULL

- 10G integrated stack ultra-low latency edition
- Integrated into nxFramework & nxAccess
- Greater flexibility – TCP and UDP on the fly
- Ultimate performance (Zero clock delay)
- Used on all major exchanges for the last 10 years



nxFramework – Cores / Software / Workflow

NEW

Application Layer (Hardware + Software)

nxFramework add-ons (FIX, OE stack...)
Reference designs (T2T, risk checks...)

Utility Cores (MM, ST and Math)

Streaming bus manipulation
Memory Mapped & math functions

Connectivity Cores + Software Libraries

MAC/PCS, TCP, UDP, PCIe DMA
C++ libraries & Linux drivers

Configuration Files + Build Workflow Scripts

YAML IO/frequency configuration
Project workflow Python scripts

Board Support Package (BSP)

AMD Alveo, Bittware XUP,
Arista 7130



nxFramework Board Support

» AMD Alveo™ UL3524

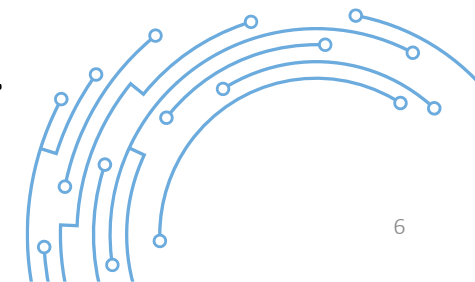
- GTF tuning for (MAC/PCS/PMA) for JAT support
- Init and sequencing characterized for best stability
- Support for disconnect
- Support for extended connectors

» Supported boards

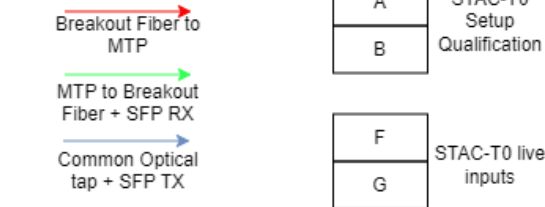
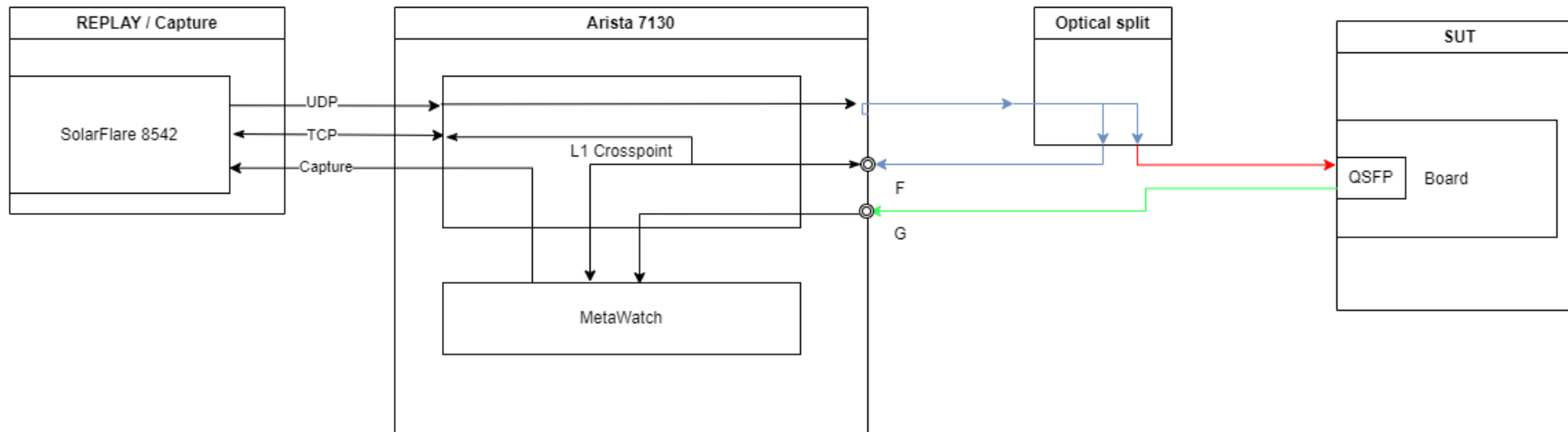
- AMD Alveo U200/U250/U50/U55C
- Bittware XUP family
- Arista 7130 switches

» nxFramework is hardware agnostic

- **Flexibility** – Ability to switch between boards
- **Time-to-market** – Rely on proven technology to get to production faster
- **Scalability** – Focus on what's important for your business. Ability to do more with less.



STAC-T0 Benchmark



SUT = Board + QSFP

**SUT latency =
G – F – (B – A) – (11cm MTA loopback)**

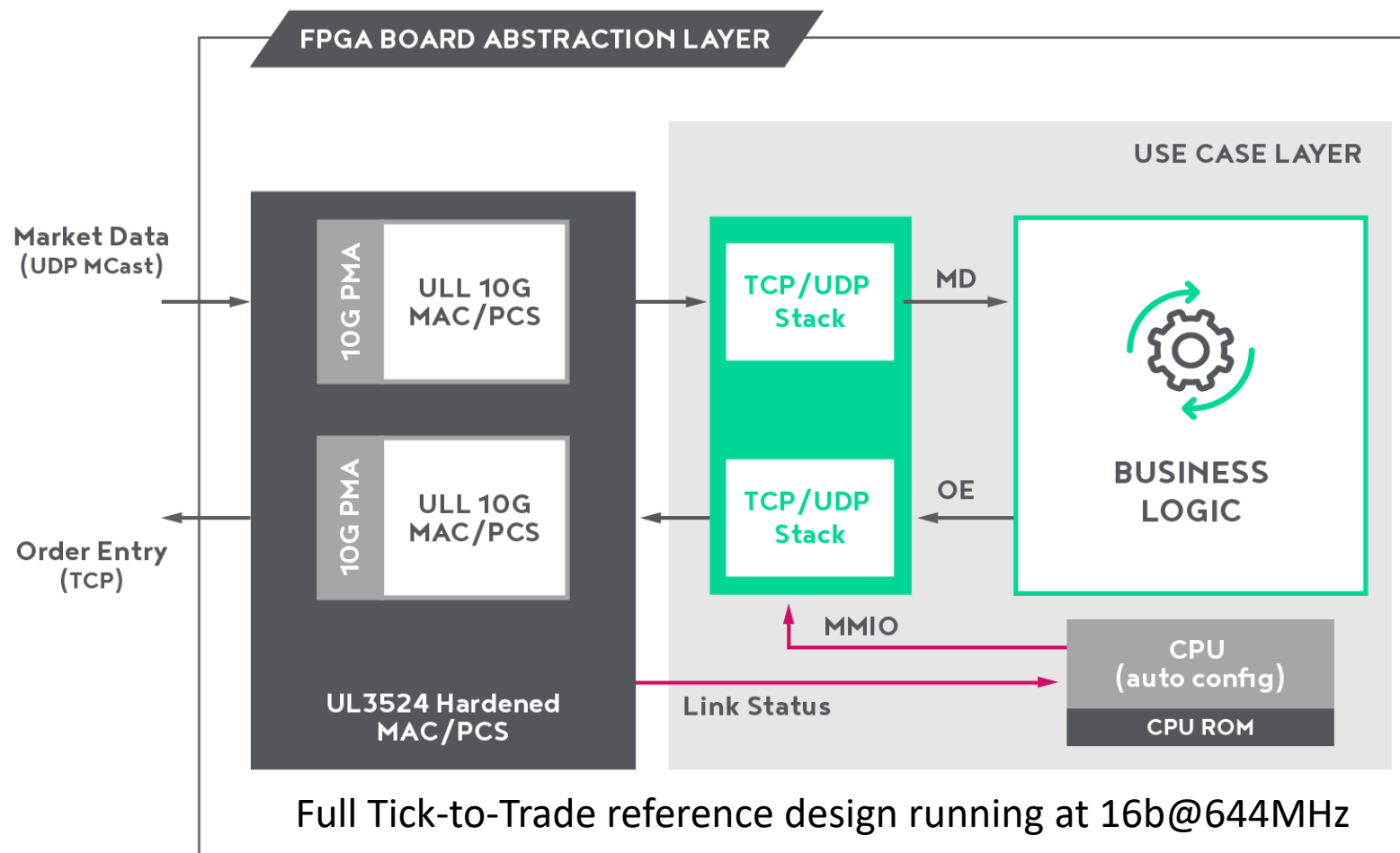
» Exegy's measurement setup:

- Based on independent sub-nano time-stamping achieving 150ps to 250ps uncertainty
- Using off-the-shelf equipment from independent 3rd party
 - (ARISTA MetaWatch & AMD Solarflare NIC)
- Using nxFramework FPGA Tick to Trade reference design
- No additional IPs necessary, run 100% on FPGA
- Validated by AMD & STAC (*report not yet published*)

STAC-T0 benchmark

UL3524 STAC-T0 Reference Design

*not an official STAC benchmark



Tick to trade latency
13.883 ns *

» **13.883ns** = Exegy T2T + GTF + Preamble Serialization (6.4ns) + QSFP & PCB traces*



Thank you!

Please tick the Exegy box for more information